(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 425 691 A1**

(12) # EUROPEAN PATENT APPLICATION published in accordance with Art. 158(3) EPC

(21) Application number: 90906376.0

(51) Int. Cl.5: H01L 23/48, H01L 23/50

(22) Date of filing: 26.04.90

(86) International application number:
PCT/JP90/00549

(87) International publication number:
WO 90/13914 (15.11.90 90/26)

(30) Priority: 01.05.89 JP 51882/89 U
01.05.89 JP 51883/89 U

(43) Date of publication of application:
08.05.91 Bulletin 91/19

(84) Designated Contracting States:
DE FR GB IT

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(54) # LEAD FRAME FOR SEMICONDUCTOR DEVICES.

(57) A lead frame of a sealed-type semiconductor device of large scale integration which has many input/output pins and which operates at high speeds. The lead frame is made of magnetic material, and its portion to be within the package has a 1 μm or thicker nonmagnetic metal coating of good conductor of electricity. This coating covert the upper surface (1a), lower surface (1b), both side surfaces (1c) and the inner end surface (1d) of the portion within the package. When the lead frame is thus formed, the inductance decreases conspicuously at the lead portions, and reliability is improved in regard to high-speed operation of the semiconductor device.

EP 0 425 691 A1

FIG. 1

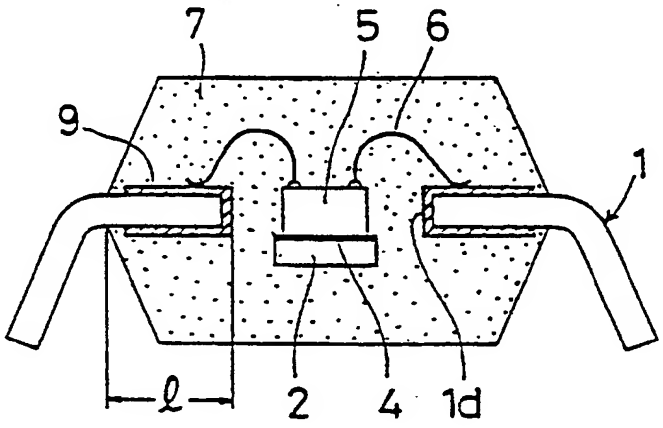
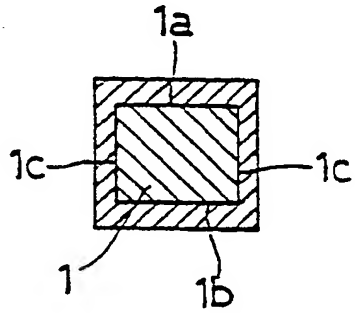


FIG. 3



LEAD FRAME FOR SEMICONDUCTOR DEVICE

Technical Field

This invention relates to a resin-sealed type, high-density semiconductor device having a large number of input/output pins (leads) and capable of operating at high speed.

Background Art

A semiconductor device (or chip) having predetermined functions are generally sealed in a package by hermetic sealing or resin sealing method for stable maintenance of its desired characteristics, thermal or electrical derivation, insulation between electrodes and convenience of transportation and handling.

A package most often used for this purpose is a resin-sealed type. This is due to the fact that this type of package is superior in mass-productivity as well as from an economical viewpoint to metal or ceramic packages and that its reliability and utility are better as a result of various improvements.

On the other hand, a glass-sealed type, mainly made of ceramics, has as good heat dissipation properties and hermetic tightness as multi-layered ceramic packages (MLCP) and thus it is suitable for enveloping chips which handle high-speed signals or chips whose heat buildup is remarkable. Furthermore, it is cheaper than an MLCP. In particular, it has an advantage that the number of leads can be increased because its four sides can be used, and it is used increasingly with increase in the demand for microcomputers which require thinner chips.

Lead frame materials currently used for these packages can be classified into an Fe-Ni group, a Cu group, an Fe group and so on. Of the above three groups, the Fe-Ni group material is preferred, depending on the purpose of use, especially if high reliability is required for the IC themselves.

The Fe-Ni group lead frames are ordinarily covered with a metal film to facilitate assembling such as chip bonding and wire bonding. Such a film is of gold or silver in case of the resin-sealed type and aluminum in case of the glass-sealed type. These materials are used selectively taking into account the degree of reliability required for IC's, the manner in which Si chips are mounted, and the cost.

Next, the prior art will be described, taking the resin-sealed type as an example.

Figs. 4 and 5 show sections of a conventional resin-sealed type semiconductor device (IC package). As shown in the figures, gold or silver films 4 are formed on a die pad portion 2 and inner pad portions 3 of a lead frame 1 in a spot-like manner. This IC package is made by mounting a semiconductor element such as an Si chip 5 on the die pad portion 2 through the film 4, electrically connecting the chip 5 and the inner pad portions 3 of the lead frame by means of gold wires 6, and by forming a resin sealing 7. To assure good bonding properties between the chip 5 and the wire 6, the metal film 4 is provided only on their bonding portion.

Numeral 8 designates a plating layer of tin or solder formed on the surface of an outer lead. This plating layer 8 is provided because if the lead frame is made of an Fe-Ni alloy or the like, its wettability with solder or the like is extremely bad and it is necessary to solder the frame to a printed circuit board or the like with high reliability.

Since a lead made of an Fe-Ni alloy is a magnetic material, its self-inductance tends to be big during use of the device. Especially in case of a high-density semiconductor device having a greater number of input and output pins, the length of the lead portion inside the resin tends to be long and thus the self-inductance increases remarkably. This will hamper high-speed operation of the semiconductor device.

It is an object of this invention to provide a lead frame for a semiconductor device which obviates the above-said shortcomings.

With this arrangement, the inductance of the lead frame can be reduced remarkably. For example, a lead frame made of an Fe-42%Ni alloy and having a thickness of 0.15 mm and a lead width of 0.2 - 0.12 mm has inductance values as shown in Table 1. The aluminum layer used was 5 - 10 microns thick at top and bottom of the lead frame.

As is apparent from Table 1, when the aluminum layer is less than 1 micron thick at both sides, it hardly serves to reduce the inductance. But when it is 1 micron thick or more, its effect increases remarkably.

For normal operation of a high-density integrated circuit, the inductance of the lead frame should be kept to 60 nH or less. In view of this, the effect of the present invention will exhibit most remarkably if the length of the unexposed portion of the lead frame is 10 mm or more or if the lead frame is made of a

material whose inductance tends to increase easily. The alloy material for the lead frame may be iron-nickel alloy containing 38 - 55 percent by weight of nickel, or iron-nickel-cobalt alloy containing 25 - 35 percent by weight of nickel and 15 - 25 percent by weight of cobalt.

In the preferred embodiment, the lead frame is covered at its unexposed portion with aluminum. But it was found that the self-inductance can be reduced effectively when covered with any other non-magnetic metal having a good electrical conductivity such as an aluminum alloy, copper, gold, silver, zinc, lead, tin or their alloy.

According to this invention, the covering layer of a non-magnetic metal having a good conductivity is provided over the top and bottom surfaces and side surfaces of the portion of the magnetic lead frame where it is not exposed while in use. By giving a thickness of 1 micron or more at its sides, the inductance at the lead portion can be reduced remarkably. This makes it possible to improve the reliability of a high-density semiconductor device which has many input/output pins and is operated at a high speed.

Brief Description of the Drawings

Figs. 1 and 2 are sectional views of embodiments according to this invention showing one form of use. Fig. 3 is a sectional view of the lead at the resin-sealed portion of the same, and Figs. 4 and 5 are sectional views of a prior art resin-sealed type semiconductor device.

Best Mode for Embodying the Invention

One embodiment of this invention will be described with reference to Figs. 1 to 3.

The elements designated 1, 2 and 4 - 7 in Figs. 1 and 2 are the same as those in Figs. 4 and 5. The metal films 4 in Fig. 1 are made of silver whereas the films 4 in Fig. 2 are made of gold. In both of the embodiments, covering layers 9 made of a non-magnetic metal having a good conductivity are provided on the entire surfaces of the portion of the lead frame 1 where it is covered with the resin sealing 7 (excepting the die pad portion 2), i.e. top surface 1a, bottom surface 1b, both side surfaces 1c (Fig. 3) and inner end faces 1d. In the first embodiment shown in Fig. 1, layers 9 are of aluminum whereas in the second embodiment shown in Fig. 1, the layers 9 are of aluminum whereas in the second embodiment shown in Fig. 2, they are of copper. Also, the covering layers 9 are one micron thick or more at the portions 1c in both embodiments shown in Figs. 1 and 2. Both in Figs. 1 and 2, the plating layers of tin or solder on the outer leads are not shown.

Next, in order to verify these effects, the following experiments were conducted.

(Experiment 1)

A 35 mm x 35 mm flat mold package having the structure shown and having leads extending in four directions were prepared. The minimum lead length ℓ at the sealed portion was 10 mm while the maximum length was 15 mm. The aluminum covering layers 9 shown in Fig. 1 were six microns thick at the top and bottom surfaces and one micron thick at the sides.

For comparison sake, a semiconductor device similar to the above device was prepared by use of a typical prior art lead frame (with aluminum coverings provided on only the top surfaces within the range of 3 mm from the end).

The inductance was measured for each of these devices. The inductance at 100 kHz was 80 - 125 nH with the prior art structure whereas with that of the specimen according to the present invention it was 28 - 42 nH, which is low enough to assure correct operation of the device.

(Experiment 2)

An Fe-42%Ni lead frame 0.2 mm wide and 0.1 mm thick with the length of the unexposed portion of 10 mm was prepared.

In this state, the inductance of this lead frame was 73 nH at 1 MHz. Then, this lead frame was covered with the an aluminum layer 6 having a thickness of 6 microns at top and bottom surfaces and 1 micron at both sides. The inductance at 1 MHZ dropped to 12 nH.

The effects of this invention will be apparent from the results of these experiments.

In the drawings, the lead frame is used for a resin-sealed type semiconductor device. But the same effects can be expected when it is used for a glass-sealed type semiconductor device, too.

Table 1

	Inductance (nH) (100kHz)					
Lead length (mm)	Without Aℓ	Aℓ on one side	Aℓ on upper, lower and side surfaces			
			0μm on side	0.5μm on side	1μm on side	2μm on side
3	26± 3	19± 3	13± 3	12± 3	7± 3	6± 3
5	44± 3	31± 3	22± 3	21± 3	13± 3	11± 3
10	87± 3	62± 3	44± 3	42± 3	25± 3	21± 3
15	130± 3	93± 3	66± 3	63± 3	40± 3	32± 3
20	170± 3	120± 3	88± 3	85± 3	51± 3	42± 3
25	220± 3	160± 3	110± 3	105± 3	62.5± 3	53± 3

Claims

1. A lead frame for a semiconductor device, said lead frame being made of a magnetic material and provided over the entire area on the top and bottom surface and both sides thereof at its unexposed portion (where it is located within a package of said semiconductor device) with convering layers made of a non-magnetic metal having a high conductivity, said layers being 1 micron thick or more at both sides, whereby reducing the self-inductance of each lead.

2. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is aluminum or an aluminum alloy.

3. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is copper or a copper alloy.

4. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is gold or a gold alloy.

5. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is silver or a silver alloy.

6. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is zinc or a zinc alloy.

7. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said

covering layers is lead or a lead alloy.

8. A lead frame for a semiconductor device as claimed in claim 1, wherein said metal forming said covering layers is tin or a tin alloy.

9. A lead frame for a semiconductor device as claimed in any of claims 1 - 8, wherein said lead frame is made of an iron-nickel alloy containing 38 - 55 percent by weight of nickel or an iron-nickel-cobalt alloy containing 25 - 35 percent by weight of nickel and 15 - 25 percent by weight of cobalt.

10. A lead frame for a semiconductor device as claimed in any of claims 1 - 9, wherein the length of said unexposed portion is 10 mm or more.

FIG. 1

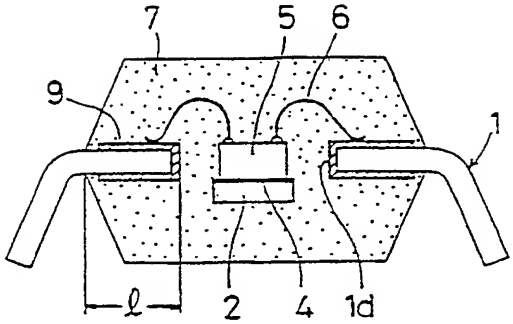


FIG. 3

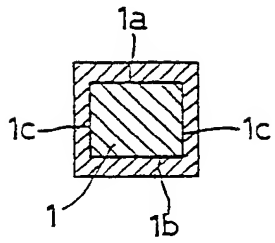


FIG. 2

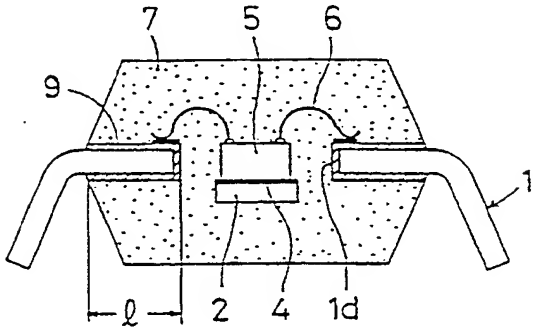


FIG. 5

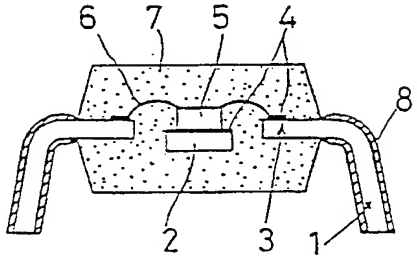
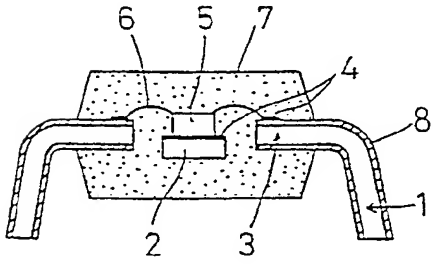


FIG. 4



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP90/00549

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H01L23/48-23/50

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H01L23/48-23/50

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

Jitsuyo Shinan Koho	1926 - 1989
Kokai Jitsuyo Shinan Koho	1971 - 1989

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	JP, A, 60-77450 (Hitachi Cable, Ltd.), 2 May 1985 (02. 05. 85), (Family: none)	1 - 10

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
July 16, 1990 (16. 07. 90)	July 30, 1990 (30. 07. 90)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	

Form PCT/ISA/210 (second sheet) (January 1985)

Office européen des brevets

RAPPORT DE RECHERCHE EUROPEENNE

Numéro de la demande
EP 01 20 0754

DOCUMENTS CONSIDERES COMME PERTINENTS

Catégorie	Citation du document avec indication, en cas de besoin, des parties pertinentes	Revendication concernée	CLASSEMENT DE LA DEMANDE (Int.Cl.7)
A	EP 0 425 691 A (SUMITOMO ELECTRIC INDUSTRIES) 8 mai 1991 (1991-05-08) * page 3, ligne 53 - page 4, ligne 12 *	1-10	G04C10/00
A	US 5 569 545 A (ENDO YASUHIRO ET AL) 29 octobre 1996 (1996-10-29) * colonne 5, ligne 22-64 *	1-10	

DOMAINES TECHNIQUES RECHERCHES (Int.Cl.7)

G04C
H05K
G04D

Le présent rapport a été établi pour toutes les revendications

Lieu de la recherche	Date d'achèvement de la recherche	Examinateur
LA HAYE	18 septembre 2001	Exelmans, U

CATEGORIE DES DOCUMENTS CITES

X : particulièrement pertinent à lui seul
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EPO FORM 1503 03.82 (P04C02)

ANNEXE AU RAPPORT DE RECHERCHE EUROPEENNE RELATIF A LA DEMANDE DE BREVET EUROPEEN NO. EP 01 20 0754

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18-09-2001

Document brevet cité au rapport de recherche	Date de publication	Membre(s) de la famille de brevet(s)	Date de publication
EP 0425691 A	08-05-1991	EP 0425691 A1	08-05-1991
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		JP 3072661 A	27-03-1991
		US 5134459 A	28-07-1992
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EPO FORM P0460

Pour tout renseignement concernant cette annexe : voir Journal Officiel de l'Office européen des brevets, No.12/82

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 20 0754

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 7)
A	EP 0 425 691 A (SUMITOMO ELECTRIC INDUSTRIES) 8 May 1991 (1991-05-08) *page 3, line 53 - page 4, line 12* ---	1-10	G04C10/00
A	US 5 569 545 A (ENDO YASUHIRO ET AL) 29 October 1996 (1996-10-29) *column 5, line 22-64* ---	1-10	

TECHNICAL FIELDS SEARCHED (Int. Cl. 7)

G04C
H05K
G04D

The present report has been established for all the claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 September 2001	Exelmans, U

CATEGORY OF CITED DOCUMENTS

X : Particularly relevant if taken alone
Y : Particularly relevant if combined with another
A : technological background
O : Non-written disclosure
P : Intermediate document

T : Theory or principle underlying the invention
E : Earlier patent document but published on the filing date or after that date
D : Cited in the application
L : Cited for other reasons

.....

& : Member of the same patent family, corresponding document

ANNEX TO THE EUROPEAN SEARCH REPORT RELATING TO EUROPEAN PATENT APPLICATION NO EP 01 20 0754

This annex lists the patent family members relating to the patent documents cited in the above-mentioned search report.
The members are as contained in the European Patent Office EDP filed on
The particulars are given for the purpose of information and do not involve the responsibility of the European Patent Office

18-09-2001

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP 0425691 A	08-05-1991	EP	0425691 A1	08-05-1991
		WO	9013914 A1	15-11-1990
		JP	3072661 A	27-03-1991
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